We claim:

1. A method of forming a copper interconnect on a substrate, comprising:

(a) providing a substrate with a dielectric layer formed thereon;

(b) forming a pattern comprised of at least one opening having a low pattern density in a first region and at least one opening having a high pattern density in a second region in said dielectric layer, each of said openings having sidewalls and a bottom;

(c) depositing a conformal diffusion barrier layer on said dielectric layer and on the sidewalls and bottom of said openings and depositing a first copper layer on the diffusion barrier layer that fills said openings;

(d) performing a first planarization process that removes the first copper layer and diffusion barrier layer above the dielectric layer and forms a dished upper surface on the planarized first copper layer in said openings, said planarized first copper layer has a first thickness;

(e) forming a second copper layer on said planarized first copper layer by a selective deposition process, said second copper layer extends to a level above said dielectric layer;

(f) annealing said planarized first copper layer and said second copper layer; and

(g) performing a second planarization process so that the second copper layer becomes coplanar with said dielectric layer and wherein the planarized and annealed second copper layer has a second thickness and a grain density G_{D2} and the planarized and annealed first copper layer has a grain density G_{D1}.

2. The method of claim **1** wherein said dielectric layer is comprised of SiO_2, borophosphosilicate glass, or a low k dielectric material that is fluorine doped SiO_2, carbon doped SiO_2, a poly(arylether), a polysilsesquioxane, benzocyclobutene, or a fluorinated polyimide and has a thickness of about 3000 to 7000 Angstroms.

3. The method of claim **1** wherein said substrate is comprised of an upper etch stop layer with a thickness of about 100 to 2000 Angstroms and the openings formed in said dielectric layer extend through said etch stop layer.

4. The method of claim **1** wherein said diffusion barrier layer is Ta, TaN, Ti, TiN, W, WN, or TaSiN and has a thickness between about 10 and 1000 Angstroms.

5. The method of claim **1** wherein an opening is comprised of a via, trench, or a trench formed above a via and wherein the width of said openings ranges from about 0.1 microns to over 10 microns.

6. The method of claim **1** wherein said openings formed in said first region and said openings formed in said second region have equivalent widths.

7. The method of claim **1** wherein the process of depositing said first copper layer comprises a first step of forming a copper seed layer on said diffusion barrier layer by a physical vapor deposition (PVD) or ionized metal plasma (IMP) process and a second step of depositing copper to fill said opening by a PVD, electroplating, or an electroless plating method.

8. The method of claim **1** wherein said first planarization process is a chemical mechanical polish (CMP) step.

9. The method of claim **1** wherein said second copper layer is formed by a selective electroless plating or electrochemical deposition process.

10. The method of claim **9** wherein said electroless plating process is comprised of treating said substrate with an aqueous solution having a pH of about 8 to 13 and a temperature of about 67°C to 73°C and comprised of the following: $CuSO_4 \cdot 5H_2O$ with a concentration of 10 grams per liter (g/L), a 37% formaldehyde solution in water at a concentration of 15 ml/L, EDTA with a concentration of 28 g/L, tetramethylammonium hydroxide (TMAH) with a concentration of 125 g/L, KOH with a concentration of 18.5 g/L, and 2,2-bipyridine at a concentration of 1.5 g/L.

11. The method of claim **1** wherein said annealing process is performed by heating said substrate in an oven at a temperature of about 150°C to 300°C in an inert atmosphere comprised of N_2, Ar, or H_2 for a period of about 10 seconds to 5 minutes.

12. The method of claim **1** wherein said second planarization process is a CMP buffing step involving a down force of about 2 to 4 psi and a slurry comprised of SiO_2, H_2O, and a basic component which is NaOH, KOH or NH_4OH.

13. The method of claim **1** wherein the planarized first copper layer has a thickness equal to or greater than the thickness of the planarized second copper layer.

14. The method of claim **1** wherein G_{D1} is greater than or equal to G_{D2}.

15. The method of claim **1** wherein the sheet resistance (Rs) for a copper interconnect comprised of the planarized and annealed first copper layer and the planarized and annealed second copper layer is nearly independent of the pattern density of the region in which said copper interconnect is formed.

16. The method of claim **1** wherein the Rs for a copper interconnect comprised of the planarized and annealed first copper layer and the planarized and annealed second

copper layer is nearly independent of the width of the opening in which said copper interconnect is formed.

17. A method of forming a copper interconnect on a substrate, comprising:

(a) providing a substrate with a dielectric layer formed thereon;

(b) forming at least one opening having a first width in a first region in said dielectric layer and at least one opening having a second width that is unequal to said first width in a second region in said dielectric layer, each of said openings having sidewalls and a bottom;

(c) depositing a conformal diffusion barrier layer on said dielectric layer and on the sidewalls and bottoms of said openings and depositing a first copper layer on the diffusion barrier layer that fills said openings;

(d) performing a first planarization process that removes the first copper layer and diffusion barrier layer above the dielectric layer and forms a dished upper surface on the planarized first copper layer in said openings, said planarized first copper layer has a first thickness;

(e) forming a second copper layer on the planarized first copper layer by a selective deposition process, said second copper layer extends to a level above said dielectric layer;

(f) annealing the planarized first copper layer and said second copper layer; and

(g) performing a second planarization process so that the second copper layer becomes coplanar with said dielectric layer and wherein the planarized and annealed second copper layer has a second thickness and a grain density G_{D2} and the planarized and annealed first copper layer has a grain density G_{D1}.

18. The method of claim **17** wherein said dielectric layer is comprised of SiO_2, borophosphosilicate glass, or a low k dielectric material that is fluorine doped SiO_2, carbon doped SiO_2, a poly(arylether), a polysilsesquioxane, benzocyclobutene, or a fluorinated polyimide and has a thickness of about 3000 to 7000 Angstroms.

19. The method of claim **17** wherein said substrate is further comprised of an upper etch stop layer with a thickness of about 100 to 2000 Angstroms and the openings formed in said dielectric layer extend through said etch stop layer.

20. The method of claim **17** wherein said diffusion barrier layer is Ta, TaN, Ti, TiN, W, WN, or TaSiN and has a thickness between about 10 and 1000 Angstroms.

21. The method of claim **17** wherein the width of said openings ranges from about 0.1 microns to over 10 microns.

22. The method of claim **17** wherein the process of depositing said first copper layer comprises a first step of forming a copper seed layer on said diffusion barrier layer by a PVD or IMP process and a second step of depositing copper to fill said opening by a PVD, electroplating, or electroless plating method.

23. The method of claim **17** wherein said first planarization process is a chemical mechanical polish (CMP) step.

24. The method of claim **17** wherein said second copper layer is formed by a selective electroless plating or electrochemical deposition process.

25. The method of claim **24** wherein said electroless plating process is comprised of treating said substrate with an aqueous solution having a pH of about 8 to 13 and a temperature of about 67°C to 73°C and comprised of the following: $CuSO_4{\cdot}5H_2O$ with a concentration of 10grams (g)/liter (L); a 37% formaldehyde solution in water with a

concentration of 15 ml/L; EDTA with a concentration of 28 g/L; tetramethylammonium hydroxide (TMAH) at a concentration of 125 g/L; KOH with a concentration of 18.5 g / L; and 2,2-bipyridine with a concentration of 1.5 g/L.

26. The method of claim **17** wherein said annealing process is performed by heating said substrate in an oven at a temperature of about 150°C to 300°C in an inert atmosphere comprised of N_2, Ar, or H_2 for a period of about 10 seconds to 5 minutes.

27. The method of claim **17** wherein said second planarization process is a CMP buffing step involving a down force of about 2 to 4 psi and a slurry comprised of SiO_2, H_2O, and a basic component which is NaOH, KOH or NH_4OH.

28. The method of claim **17** wherein the planarized first copper layer has a thickness equal to or greater than the thickness of the planarized second copper layer.

29. The method of claim **17** wherein G_{D1} is greater than or equal to G_{D2}.

30. The method of claim **17** wherein the Rs for a copper interconnect formed in an opening in said first region is nearly equivalent to the Rs for a copper interconnect formed in an opening in said second region.

31. The method of claim **17** wherein the sheet resistance for a copper interconnect comprised of the planarized and annealed first copper layer and the planarized and annealed second copper layer is nearly independent of the pattern density of the region in which said copper interconnect is formed.

32. The method of claim **17** further comprised of forming a plurality of openings in a plurality of regions in said dielectric layer, said openings having a plurality of widths.

33. The method of claim **32** wherein the copper interconnect comprised of the planarized and annealed first copper layer and the planarized and annealed second

copper layer has a Rs that is nearly independent of the width of the opening in which said copper interconnect is formed.

34. A copper interconnect structure in a semiconductor device, comprising:

(a) a first copper layer having vertical sidewalls, a planar bottom, and a concave top surface formed in an opening in a dielectric layer on a substrate, said first copper layer has a first thickness and a grain density G_{D1}; and

(b) a second copper layer having vertical sidewalls, a substantially planar top surface that is about coplanar with the top of said dielectric layer, and a convex bottom surface that forms an interface with said concave top surface of said first copper layer, said second copper layer has a second thickness and a grain density G_{D2} and is formed in said opening in a dielectric layer on a substrate.

35. The copper interconnect of claim **34** wherein said substrate is further comprised of an upper etch stop layer and the opening extends through said etch stop layer.

36. The copper interconnect of claim **34** wherein said dielectric layer is comprised of SiO_2, borophosphosilicate glass, or a low k dielectric material that is fluorine doped SiO_2, carbon doped SiO_2, a poly(arylether), a polysilsesquioxane, benzocyclobutene, or a fluorinated polyimide.

37. The copper interconnect structure of claim **34** wherein the combined thickness of said first copper layer and said second copper layer is from about 3000 to 7000 Angstroms.

38. The copper interconnect structure of claim **34** further comprised of a conformal diffusion barrier layer formed in said opening along the sidewalls and bottom of said first copper layer and along the sidewalls of said second copper layer.

39. The copper interconnect structure of claim **34** wherein the width of said first copper layer and the width of said second copper layer have a range from about 0.1 microns to over 10 microns.

40. The copper interconnect structure of claim **34** wherein said copper interconnect has a sheet resistance that is nearly independent of the width of said first copper layer and the width of said second copper layer.

41. The copper interconnect structure of claim **34** wherein said opening is part of a pattern that includes a plurality of other openings having a pattern density and said copper interconnect has a sheet resistance (Rs) that is nearly independent of said pattern density.

42. The copper interconnect structure of claim **34** wherein the first thickness of said first copper layer is equal to or greater than the second thickness of said second copper layer.

43. The copper interconnect structure of claim **34** wherein G_{D1} is greater than or equal to G_{D2}.

44. The copper interconnect structure of claim **34** wherein said substrate is comprised of a metal layer and said first copper layer of said copper interconnect is formed above said metal layer and forms an electrical contact to said metal layer.

45. A copper interconnect formed in an opening comprised of a trench formed above a via in a dielectric layer on a substrate, said trench has sidewalls, a bottom, and a width that is larger than the width of said via and said via has sidewalls and a bottom, comprising:

(a) a first copper layer that fills said via and extends into said trench, said first copper layer has vertical sidewalls and a planar bottom in said via and vertical sidewalls and a planar bottom in said trench, a concave top surface formed within the trench, a first thickness, and a grain density G_{D1}; and

(b) a second copper layer having vertical sidewalls, a substantially planar top surface that is about coplanar with the top of said dielectric layer and the top of the trench, and a convex bottom surface that forms an interface with the concave top surface of said first copper layer, said second copper layer has a second thickness and a grain density G_{D2} and is formed within the trench portion of said opening.

46. The copper interconnect of claim **45** wherein said substrate is further comprised of an upper etch stop layer and the via extends through said etch stop layer.

47. The copper interconnect of claim **45** wherein the combined thickness of said first copper layer and said second copper layer is from about 3000 to 7000 Angstroms.

48. The copper interconnect of claim **45** further comprised of a conformal diffusion barrier layer formed along the vertical sidewalls of the first copper layer and the second copper layer and along the bottom of the first copper layer in the trench and via.

49. The copper interconnect of claim **45** wherein said copper interconnect has a sheet resistance that is nearly independent of the width of the trench.

50. The copper interconnect of claim **45** wherein said opening is part of a pattern that includes a plurality of other openings having a pattern density and said copper interconnect has a sheet resistance (Rs) that is nearly independent of said pattern density.

51. The copper interconnect of claim **45** wherein the first thickness of said first copper layer is equal to or greater than the second thickness of said second copper layer.

52. The copper interconnect structure of claim **45** wherein G_{D1} is greater than or equal to G_{D2}.